A MONOLITHIC OPERATIONAL AMPLIFIER

BY R. J. WIDLAR

I. INTRODUCTION

A high-performance DC amplifier constructed on a single silicon die is described. It is a high-gain operational-type amplifier meant for use with external feedback elements to determine operating characteristics. It is useful as a general purpose AC or DC amplifier to frequencies as high as 10 Mc.

Applications include amplifying the output of transducers such as resistive bridges, thermocouples, hall-effect devices, photodiodes, etc. With proper feedback elements it can also perform the integrating, differentiating, summing, and subtracting functions required in an analog computer. In addition, the amplifier can be used with reactive feedback elements for precise frequency shaping of the gain characteristics or with a bridged-T filter to make a band-pass amplifier. Diodes can be incorporated in the feedback loop to form low-threshold detectors and instrument rectifiers, or the amplifier can be operated open loop as a voltage comparator.

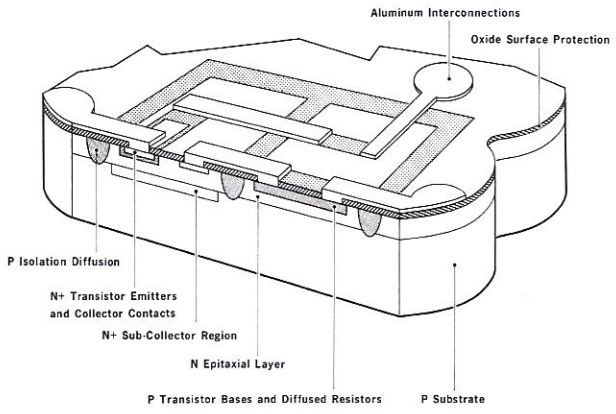

FIG. 1. Sectional view of Fairchild planar-epitaxial integrated circuit.

The amplifier takes advantage of the inherent features of monolithic construction to achieve low DC offset and low thermal drift as well as wide-band operation and low-power consumption. A planar-epitaxial manufacturing process, similar to that widely used by Fairchild Semiconductor for digital integrated circuits, is employed. A sectional view indicating the different diffusions is given in Fig. 1.

II. CIRCUIT DESCRIPTION

Design Considerations

Conventional DC amplifier designs are not easily adapted to monolithic construction. Close control of component tolerances, large resistances, circuit adjustments, and complementary transistors are generally required. With integrated circuits, tight control of absolute resistor values is difficult. Second, the temperature coefficient of diffused silicon resistors is quite high (0.1%/°C). An order of magnitude improvement in temperature coefficient can be expected using thin-film resistors at the expense of increased complexity. Third, large resistors require excessive surface area and make the integrated circuit difficult to manufacture; the same is true for large capacitors. Fourth, circuit adjustments, although possible with thin-film resistors, are time consuming, subject to irreversible error and therefore costly. Finally, the manufacture of complementary transistors on a single silicon substrate increases the number of processing steps as well as the degree of control that must be exercised over them. Even then, it is practically impossible to optimize the characteristics of both the NPN and the PNP transistors.

The distinct advantages of integrated circuitry, related to circuit design, are that it is possible to make and interconnect a relatively large number of transistors and

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moderate-value resistors without a great deal more difficulty than is encountered in manufacturing a single transistor. It is also possible to use an optimum geometry for each transistor in the circuit without affecting complexity. Further, excellent component matching is obtained throughout the circuit; and the close thermal coupling of all components ensures the matching over a wide temperature range.

The circuit to be described is unusual in that large resistances and complementary transistors were eliminated at no sacrifice in performance. In addition, the important characteristics of the amplifier are dependent only on the matching of components, rather than their absolute value. The degree of match normally available in integrated circuitry makes unnecessary any adjustments.

The active area of the integrated amplifier was minimized not only to improve high-frequency response but also to reduce the possibility of crystalline defects and surface phenomena causing failures. This will decrease manufacturing costs as well as increase reliability. The small size of the circuit is illustrated in Fig. 2, where it is compared with an early planar transistor.

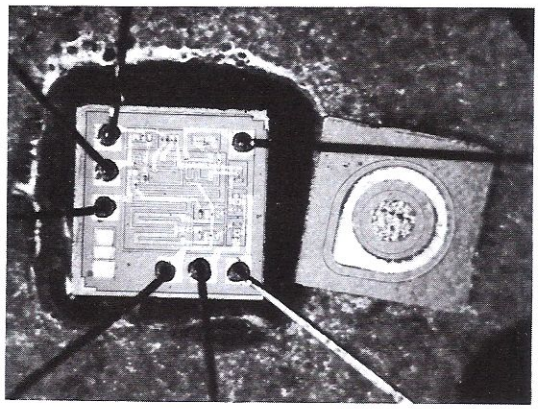


FIG. 2. Comparison of the Fairchild μA702 (left) with a 2N1613 planar transistor.

Input Stage

In general, the desirable characteristics for an input stage of a DC amplifier are low offset voltage, offset current, input current, and thermal drift. Matched differential pairs are almost universally used. With this configuration, the input bias of one active device cancels that of the other to give offset and drift dependent only on the degree of match.

In cases where offset voltage is of prime importance, the bipolar transistor is undoubtedly the best choice of an active device for the input stage. Offset voltages of a few millivolts are easily obtained over a wide temperature range. Low input currents and high input impedance can be realized by using very high-gain transistors and operating them at sufficiently low collector currents. A Darlington input stage can also be used at some sacrifice in offset voltage, thermal drift, and noise figure. Other active devices, notably the field-effect transistor, are difficult to match closer than several tens of millivolts. Low offset and drift cannot be obtained without elaborate compensation precedures. Therefore, the use of these devices is limited to cases where offset voltage is of secondary importance and an input current less than a few nanoamperes is mandatory.

It appears that the most satisfactory compromise for the input stage of a general-purpose amplifier is a matched pair of bipolar transistors operated at a low collector current. In an integrated circuit, the input-stage transistors can be matched quite easily over several decades of collector current by making them with identical structures and locating them physically close together. There is, however, a problem in obtaining the low collector currents; conventional circuit designs require large resistance values.

Much reduced resistance values can be used at the expense of input-stage gain. Some analysis of the problem shows that a low gain in the input stage can be tolerated if the second stage is well balanced. The offset of the second stage appears as an input offset divided by the gain of the input stage.

In the distribution curves obtained in manufacturing an integrated amplifier, the input-stage offset will add with the equivalent second-stage offset as the square root of the sum of squares. For example, if the gain of the input stage is two and the 90-percent point in the distribution curves for the individual input and second stage offsets is 5 mV, the 90-percent point in the distribution of complete amplifiers will be only 5.6 mV. Hence, even with this low gain, the offset contribution from the second stage is quite small.

These facts were used in the design of the input stage. The transistors are operated at 200-μA collector current, but only 2-K collector-load resistors are used. This gives an unloaded differential gain of approximately 15. Therefore, if a balanced second-stage design is employed, its contribution to input offset can be made negligible.

The differential input stage (Q_2 and Q_3) and its load resistors (R_1 and R_2) can be seen in Fig. 3. The emitters of the input stage are fed from a current source (Q_1) to obtain good input common-mode rejection. The current source is biased from a voltage divider. The V_{BE} of the current-source transistor is compensated in the divider with a diode-connected transistor (Q_9).

Second Stage

It is now necessary to design a second stage configuration that will both operate with the small DC drops across the input stage load resistors and be inherently as well balanced as the input stage. The full differential gain of the

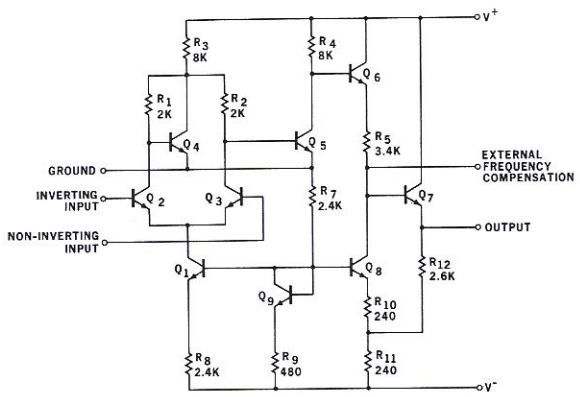


FIG. 3. Complete schematic of the amplifier.

input stage should also be used. It would also be of advantage to have a single-ended output since continuing with a differential connection to the third stage increases the number of components and creates physical layout problems on the silicon chip.

A connection which satisfies all these requirements is shown in Fig. 3. Q_4 and Q_5 are identical transistors placed close to one another. Their bases are fed from a common-voltage point through identical resistors (the input-stage load resistors, R_1 and R_2). Therefore, when the input-stage collector currents are equal, the collector currents of Q_4 and Q_5 will likewise be equal, so the second stage is balanced. Q_4 also functions as a unity gain amplifier which inverts the output of Q_2 and combines it with the output of Q_3 at the base of Q_5. Therefore, the full differential gain of the input stage is used. A single-ended output is obtained at the collector of Q_5.

An additional feature of this circuit is that under balanced conditions the single-ended output of Q_5 is insensitive to changes in positive supply voltage. If the positive supply voltage is increased, the collector currents of both Q_4 and Q_5 will increase such that the voltage on the collector of Q_5 remains constant; if this voltage does change some due to mismatches, the change is divided by a gain of roughly 1,000 before appearing in the input.

Because of the small load resistances of the input stage, the second-stage amplifier (Q_5) is essentially voltage driven. Therefore, the gain is not greatly affected by the current gain of Q_5 and is relatively constant over a wide range of operating temperatures.

Output Stage

The first two stages have provided nearly enough voltage gain for the amplifier. Since both positive and negative output swings are desired, some form of DC level shifting must be provided as the output of the second stage cannot swing negative. The usual solution to this problem is to use a PNP transistor both to give the level shifting and to provide some additional gain. In monolithic integrated circuits, however, this is not a simple answer.

A second approach to level shifting is the use of a zener diode. One problem here is that zener diodes are noisy and can appreciably affect the overall noise figure of the amplifier. Furthermore, only a single-voltage zener diode (the emitter-base junction) is usually available in the circuit.

In this amplifier an entirely new output-stage design is used to avoid these difficulties. It incorporates only NPN transistors and no zener diodes; yet its performance is comparable to designs using the best complementary transistors.

As can be seen from Fig. 3, the output of the second stage is buffered with an emitter follower, Q_6. A current source (Q_8) provides a voltage drop across R_5 which gives the basic level shifting. An additional emitter follower (Q_7) is used to give low output impedance. The load resistor of Q_7 is fed back to the emitter of Q_8 giving a controlled amount of positive feedback. Hence, the output stage actually has a gain in addition to DC level shifting. The feedback also enhances the available output swing so that it is nearly equal to the supply voltages.

To summarize the characteristics of this output stage, it has a 200-K input impedance, a 5-V DC level shift, a voltage gain of 2.5 and a 200-Ω output impedance. It can deliver a peak-to-peak symmetrical output swing of about 1.8 times the negative supply voltage.

Conditions for DC Balance

An interesting feature of the overall amplifier design is that DC balance (zero output for zero input) can be obtained independent of the supply voltages and absolute resistor values. This will be shown to hold true to a first approximation in the analysis that follows. Infinite current gains will be assumed for the transistors, as will perfect component matching in some cases. In addition, the emitter-base voltages of certain transistors will be considered equal even though they are operating at different current levels. The latter assumption is not unreasonable in an integrated circuit because the transistor geometries can be scaled in proportion to the operating current.

Using Fig. 3, the output voltage can be written as

$$V_o = V^+ - R_4 I_{C5} - R_5 I_{C8} - 2V_{BE} \qquad (1)$$

If the input-stage collector currents are equal, Q_4 and Q_5 are well matched and R_1 is equal to R_2, then I_{C4} and I_{C5} will be equal. Thus,

$$V^+ - R_3 I_{C5} - \left(R_3 + \frac{R_1}{2}\right) I_{C1} - V_{BE} = 0 \qquad (2)$$

The collector current of Q_8 is given by

$$I_{C8} = -\frac{\frac{R_9(V^- + V_{BE})}{R_7 + R_9} - \frac{R_{11}(V^- - V_o)}{R_{11} + R_{12}}}{R_{10} + \frac{R_{11}R_{12}}{R_{11}+R_{12}}} \quad (3)$$

While the collector current of Q_1 is

$$I_{C1} = -\frac{R_9(V^- + V_{BE})}{R_8(R_7+R_9)} \quad (4)$$

Substituting Eq. (3) into Eq. (1) yields

$$\left(1 - \frac{R_5R_{11}}{R_{10}R_{11} + R_{10}R_{12} + R_{11}R_{12}}\right)V_o =$$

$$V^+ - R_4I_{C5} + \frac{R_5\left(\frac{R_9}{R_7+R_9} - \frac{R_{11}}{R_{11}+R_{12}}\right)}{R_{10} + \frac{R_{11}R_{12}}{R_{11}+R_{12}}} V^-$$

$$+ \left(\frac{\frac{R_9R_5}{R_7+R_9}}{R_{10} + \frac{R_{11}R_{12}}{R_{11}+R_{12}}} - 2\right)V_{BE} \quad (5)$$

Combining Eq. (4) and Eq. (2) gives

$$V^+ - R_3I_{C5} + \frac{R_9\left(R_3 + \frac{R_1}{2}\right)}{R_8(R_7+R_9)}V^- + \left[\frac{R_3 + \frac{R_1}{2}}{R_8(R_7+R_9)} - 1\right]V_{BE} = 0 \quad (6)$$

For balanced input and second stages, as assumed, the output voltage will be given as a function of circuit parameters by the set of Eqs. (5) and (6) above. It is desired that the output voltage under this condition be zero independent of supply voltages. This can be accomplished by setting the coefficients of V^+, I_{C5} and V^- in Eq. (5) equal to the corresponding coefficients in Eq. (6). Hence, if

$$R_3 = R_4 \quad (7)$$

and

$$\frac{R_5\left(\frac{R_9}{R_7+R_9} - \frac{R_{11}}{R_{11}+R_{12}}\right)}{R_{10} + \frac{R_{11}R_{12}}{R_{11}+R_{12}}} = \frac{R_9\left(R_3 + \frac{R_1}{2}\right)}{R_8(R_7+R_9)} \quad (8)$$

Eqs. (5) and (6) can be combined to give

$$\left(1 - \frac{R_5R_{11}}{R_{10}R_{11} + R_{10}R_{12} + R_{11}R_{12}}\right)V_o =$$

$$\left[-1 + \frac{\frac{R_9R_5}{R_7+R_9}}{R_{10} + \frac{R_{11}R_{12}}{R_{11}+R_{12}}} - \frac{R_9\left(R_3 + \frac{R_1}{2}\right)}{R_8(R_7+R_9)}\right]V_{BE} \quad (9)$$

Substituting Eq. (8) into Eq. (9) yields

$$V_o = -V_{BE} \quad (10)$$

Since V_{BE} is approximately 700 mV and the open-loop gain of the amplifier is approximately 3,000, the input referred offset is roughly 0.23 mV. This is about an order of magnitude smaller than offset due to random mismatching so the output voltage at null given by Eq. (10) is essentially zero and independent of both supply voltages. Further, if every resistor in the circuit is multiplied by any constant, Eqs. (7) and (8) will not be altered. Therefore, the conditions that establish Eq. (10) are dependent only on resistor ratios—not absolute values.

Rough, order-of-magnitude calculations show that for h_{FE} greater than 30 the assumption that h_{FE} is infinite is reasonable. This has been substantiated by experimental work. The effect of current gain on offset was found to be substantially less than the offset due to other causes. In fact, the offsets produced by the different base currents tend to cancel nearly as well as the current-gain matching of various units will permit.

DC Offset and Component Matching

It was assumed previously that certain components were perfectly matched and that the ratio of all resistors was held constant. This is obviously not quite true. In this section, the effect of mismatches on offset voltage will be investigated, and a brief description of the techniques used to minimize them will be given.

First, the sensitivity of the offset voltage to deviations in resistor ratios will be considered. The simplest method of determining the relative sensitivity of the individual resistors is to change independently the value of each resistor in the circuit and measure the effect on offset. This was done with the amplifier, and the results are given in Table I. Except for R_1 and R_2, a 10-percent change in any resistor value has little effect on offset. Since the actual resistance ratios in integrated circuitry are held substantially closer than 10 percent, deviations in the resistance ratios of R_3 through R_{12} can be neglected. Of greatest importance is the matching of R_1 with R_2, rather than the other resistors, because the offsets tend to cancel if both change together, as can be seen from Table I. For this reason, these resistors have identical geometric structures, are located close together, and are made wider than other resistors.

The offset sensitivity to mismatches in transistor parameters can likewise be determined. Experimentation similar to that used to determine resistor sensitivities has shown that the matching of Q_2 with Q_3 and Q_4 with Q_5 in both current gain and emitter-base voltage clearly dominates in

TABLE I

CHANGE IN INPUT-REFERRED OFFSET VOLTAGE FOR 10-PERCENT CHANGE IN INDIVIDUAL RESISTOR VALUES

Resistor	Nominal Value (KΩ)	Change in Offset Voltage (mV)
R_1	2.0	+2.9
R_2	2.0	-2.9
R_3	8.0	-0.7
R_4	8.0	+0.5
R_5	3.4	+0.3
R_7	2.4	-0.1
R_8	2.4	+0.4
R_9	0.48	+0.1
R_{10}	0.24	-0.1
R_{11}	0.24	-0.3
R_{12}	2.6	+0.2

determining offset. Every effort was made in mask design to ensure that these pairs would be well matched. First, the devices were located as close together as possible. The small size permitted center-to-center spacings of 5 mils. Second, the distance between these transistors and elements dissipating appreciable power was maximized to eliminate thermal gradients.

III. PERFORMANCE

Monolithic amplifiers using the design described above have been built. Their performance is summarized in Table II. The inherent balance of the design is demonstrated by the low offset-voltage and thermal-drift characteristics and the excellent supply-voltage rejection.

The amplifier may be operated with practically any combination of supply voltages, within certain limits, without greatly affecting offset. The gain and output swing will, of course, be determined by the supply voltages. The indicated 2:1 ratio of positive and negative supply voltages need not be maintained. Increased output swing (up to about ±7 V) can be obtained with larger negative supply voltages. Little is gained, however, by increasing the negative supply voltage beyond 70 percent of the positive supply voltage. The voltage gain and input bias current of the amplifier are roughly proportional to the negative supply voltage.

TABLE II

TYPICAL PERFORMANCE FIGURES FOR THE FAIRCHILD μA702 INTEGRATED OPERATIONAL AMPLIFIER

(All data for 25°C ambient temperature unless otherwise indicated)

	$V^+ = 12.0$ V $V^- = -6.0$ V	$V^+ = 6.0$ V $V^- = -3.0$ V
Input Offset Voltage	2 mV	2 mV
Input Offset Current	0.7 μA	0.5 μA
Input Bias Current	4 μA	2.5 μA
Input Impedance	25 KΩ	40 KΩ
Temperature Coefficient of Input Offset Voltage		
$0°C < T_A < +125°C$	5 μV/°C	5 μV/°C
$-55°C < T_A < 0°C$	10 μV/°C	10 μV/°C
Input Common-Mode Rejection	80 db	80 db
Open-Loop Voltage Gain	2600	700
Open-Loop Bandwidth	1 Mc	1 Mc
Output Impedance	200 Ω	300 Ω
Maximum Output Swing	±5.3 V	±2.7 V
Power Input	70 mW	17 mW
Input-Referred Positive-Supply Sensitivity	50 μV/V	100 μV/V
Input-Referred Negative-Supply Sensitivity	100 μV/V	200 μV/V

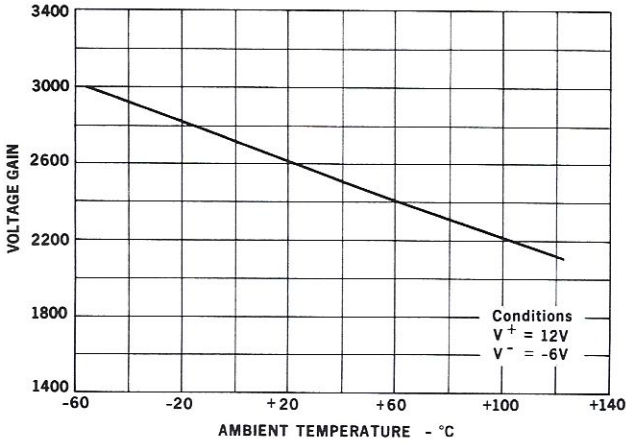


FIG. 4. Voltage gain as a function of temperature

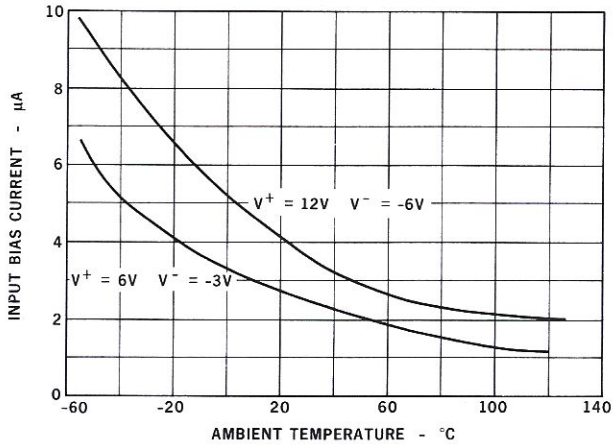


FIG. 6. Input bias current as a function of temperature.

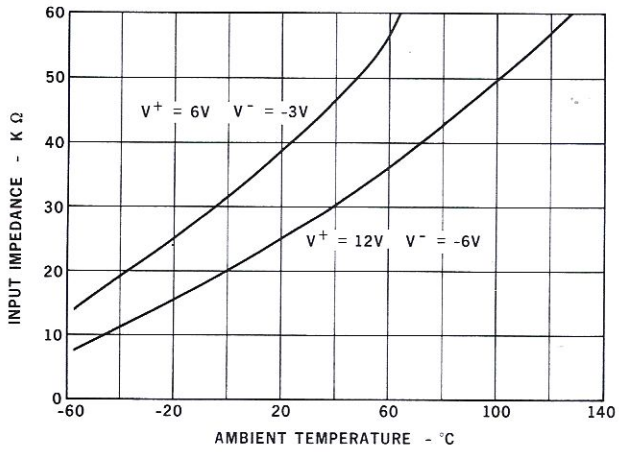


FIG. 5. Input impedance as a function of temperature.

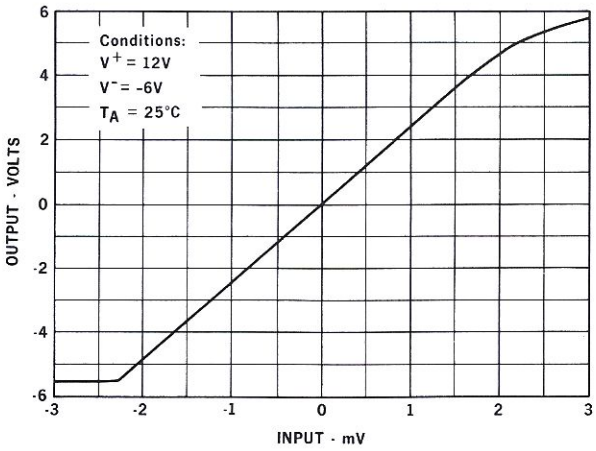


FIG. 7. Voltage transfer characteristic.

Figure 4 gives a plot of the open-loop gain as a function of temperature. The gain stays relatively constant over the entire temperature range, falling off less than 4 db at -55°C and less than 1 db at +125°C. In general, the amplifier favors high-temperature operation. Since the current gain of the transistors increases at higher temperatures, higher input impedance and lower input bias currents are obtained as shown in Figs. 5 and 6. The increased current gain also gives some improvement in balance, gain stability, and thermal drift. These facts, along with the small size of the amplifier, indicate that it is well suited to applications where a temperature-stabilizing oven is used to obtain very low drifts. Excellent performance can be obtained even if the temperature control is rather loose. Some improvement can, in fact, be obtained simply by locating the amplifier at some "hot spot" within the equipment.

The voltage-transfer characteristic of the amplifier given in Fig. 7 illustrates the output-swing capabilities and the linearity. The maximum available symmetrical output swing is plotted as a function of load resistance in Fig. 8.

The primary limitation on output swing under load is the current available from the output load resistor (R_{12}) to drive the load with negative outputs. Therefore, the swing can be improved by connecting an external resistor between the output terminal and the negative supply voltage as shown in Fig. 8. Even larger swings can be obtained if the resistor is returned to a more negative supply. Since the output impedance is quite low, considerable excess current can be drawn in this fashion without affecting offset or gain. The peak current from the output terminal should, however, be kept below 10 mA. Higher currents would cause excessive dissipation in the output transistor, thermal gradients across the silicon die, and possible thermal feedback.

The frequency response of this amplifier is of considerable importance since it is primarily intended for use as a feedback amplifier. Specifically, it is desired that the high-frequency rolloff be less than 12 db/octave at frequencies where the loop gain is greater than one. If this condition is not satisfied, the amplifier will oscillate when feedback is applied.

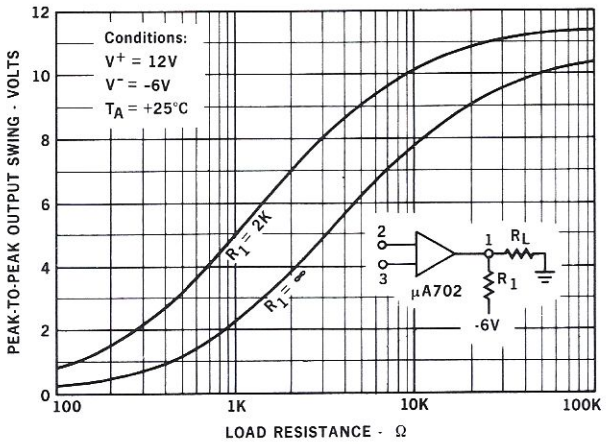


FIG. 8. Maximum output swing as a function of load resistance.

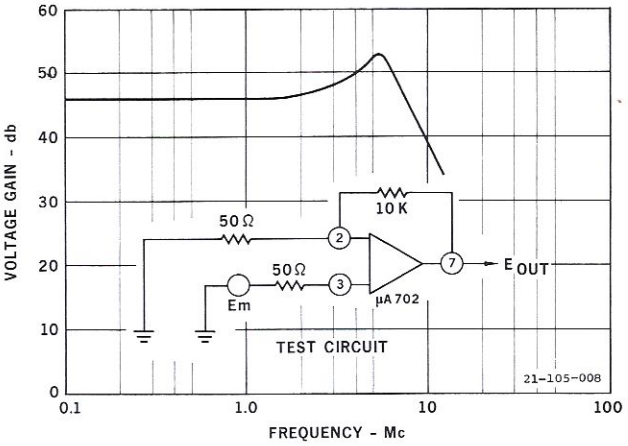


FIG. 10. Closed-loop frequency response of "x200" amplifier without external frequency compensation.

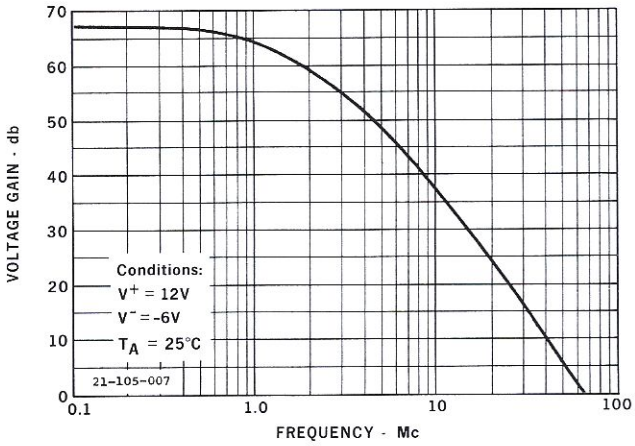


FIG. 9. Open-loop frequency response.

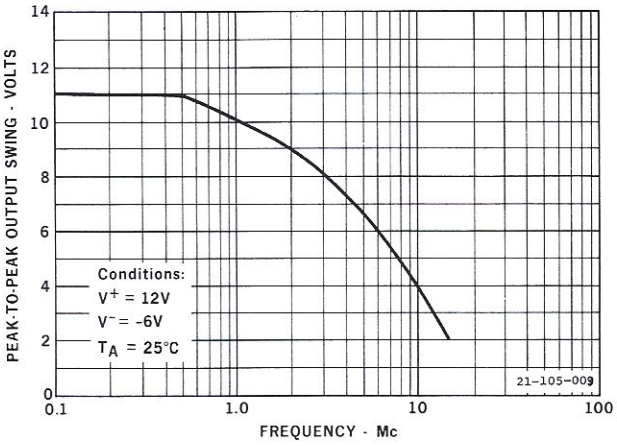


FIG. 11. Maximum output voltage swing as a function of frequency.

The open-loop frequency response of the amplifier is plotted in Fig. 9. The high-frequency rolloff approaches 12 db/octave at 7 Mc for an open-loop gain of somewhat less than 46 db. Therefore, the amplifier is stable for closed-loop gains down to 46 db. To illustrate the point, a typical circuit for a 46-db amplifier is shown in Fig. 10 along with the closed-loop frequency response. If lower closed-loop gains are desired, external frequency compensation must be added. Details on frequency compensation are given in Section IV.

As shown in Fig. 10, the bandwidth of the amplifier is extended by the application of feedback. However, the full output swing of the amplifier cannot be obtained over this extended frequency range. The basic frequency limitations of output swing are indicated in Fig. 11.

The input common-mode rejection ratio of the amplifier is also frequency limited, as indicated in Fig. 12. The plot shows that excellent common-mode rejection can be obtained at frequencies above 1 Mc if low source resistances are used.

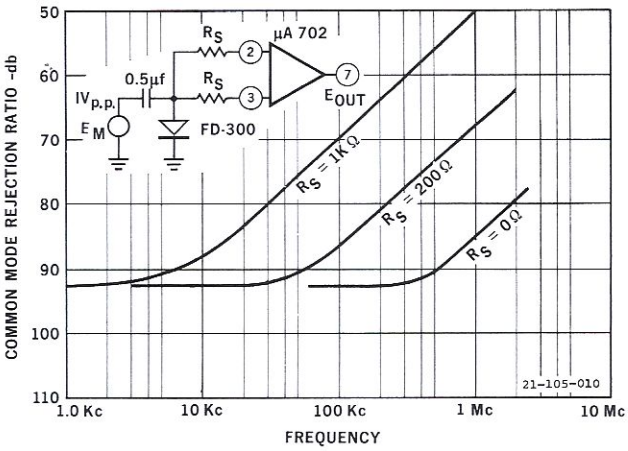
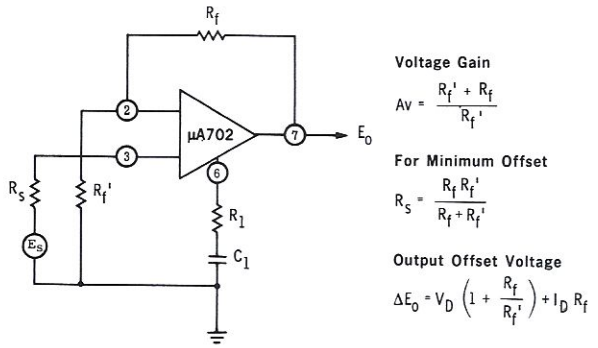


FIG. 12. Common mode rejection ratio as a function of frequency for various source resistances. Fairchild μA702 — typical.

IV. APPLICATIONS

Basic Feedback Circuits

One of the advantages of this type of amplifier is that large amounts of feedback can be used. Therefore, the overall performance can be made practically independent of the characteristics of the amplifier and almost totally dependent on feedback resistors. The most commonly used feedback configurations are shown in Figs. 13 and 14. These are simple voltage amplifiers.



Voltage Gain

$$Av = \frac{R_f' + R_f}{R_f'}$$

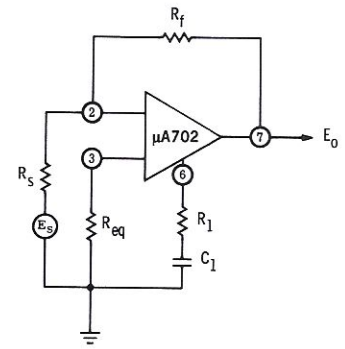
For Minimum Offset

$$R_s = \frac{R_f R_f'}{R_f + R_f'}$$

Output Offset Voltage

$$\Delta E_o = V_D \left(1 + \frac{R_f}{R_f'}\right) + I_D R_f$$

FIG. 13. Single-ended non-inverting amplifier.



Voltage Gain

$$A_V = \frac{R_f}{R_s}$$

For Minimum Offset

$$R_{eq} = \frac{R_f R_s}{R_f + R_s}$$

Output Offset Voltage

$$\Delta E_o = V_D \left(1 + \frac{R_f}{R_s}\right) + I_D R_f$$

FIG. 14. Single-ended inverting amplifier.

For the circuit in Fig. 13, the voltage gain with feedback (closed loop) is given by

$$A_V = \frac{E_o}{E_s} = \frac{A'}{1 + \left(\frac{R_f'}{R_f + R_f'}\right) A'} \tag{11}$$

where

$$A' = \left(\frac{R_{in}}{\frac{R_f R_f'}{R_f + R_f'} + R_s + R_{in}}\right) A_{vo} \tag{12}$$

A_{vo} is the voltage gain without feedback (open loop), and R_{in} is the open-loop input resistance.

A similar expression can be obtained for the circuit in Fig. 14:

$$A_V = \frac{E_o}{E_s} = \frac{-A'}{\frac{R_s}{R_f} A' + 1} \tag{13}$$

where

$$A' = \left[\frac{\frac{R_{in} R_f}{R_f + R_s}}{\frac{R_f R_s}{R_f + R_s} + R_{eq} + R_{in}}\right] A_{vo} \tag{14}$$

For closed-loop gains less than about 100 and with source resistances less than a few thousand ohms, the open-loop gain can be assumed to be infinite with less than a few percent error. If this is done, the simplified expressions in Figs. 13 and 14 can be used to compute gain.

Conditions are also given in the figures for minimum DC offset. They are based on the fact that if the two input terminals operate from equal DC resistances, the effect of the input currents will be cancelled; and only the offset current will contribute to the output offset. Equations for the output offset voltage (ΔE_o) are given as functions of the input offset voltage (V_D), input offset current (I_D), and the feedback resistors.

In these circuits, the improvement in linearity and gain stability obtained over the basic amplifier is A'/A_V, which is approximately equal to A_{vo}/A_V. For example, if the open-loop nonlinearity of the amplifier is 5 percent, the nonlinearity for a gain of 25 will be 0.05 percent.

In DC amplifier applications where offset must be held to a minimum, the circuits in Figs. 13 and 14 are most properly used as voltage and current amplifiers respectively. For example, when the input impedance of the amplifier must be considerably higher than the source resistance (R_s), the circuit in Fig. 13 would be best. If the circuit in Fig. 14 were used, large feedback resistances would be required to obtain the high input impedances. The circuit in Fig. 13 inherently has a high input impedance given by

$$R_{in}' = \frac{A'}{A_V} R_{in} \tag{15}$$

and it does not require large feedback resistances. As can be seen from the offset equations, the output offset due to input offset current is proportional to the feedback resistor (R_f), so the lower feedback resistances that could be used with the circuit in Fig. 13 would give a considerable reduction in offset.

On the other hand, if the source resistance (R_s) is high and the input impedance of the amplifier must be substantially

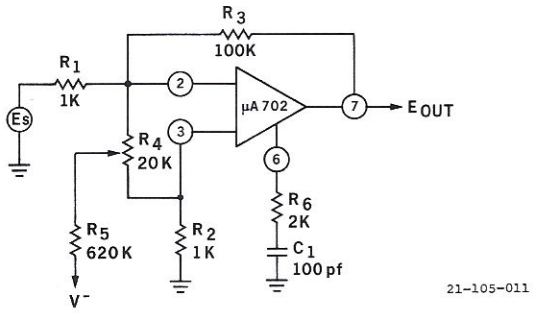
lower, the circuit in Fig. 14 would work best. If an attempt were made to shunt the source with a low resistance and use the amplifier in Fig. 13, a rather large voltage gain would be required so that the input offset voltage could be amplified. However, the circuit in Fig. 14 has a very low input impedance given by

$$R_{in}' = \frac{R_{in}}{A'} \tag{16}$$

The voltage gain in this connection would be much smaller so the output offset due to input offset voltage would be greatly reduced.

It is possible to obtain near-zero offsets by using some form of balancing with the amplifier. Circuits for doing this are shown in Fig. 15.

(a)



(b)

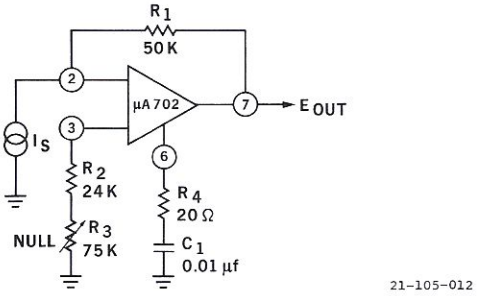


FIG. 15. Typical circuits for balancing offset of the amplifier.

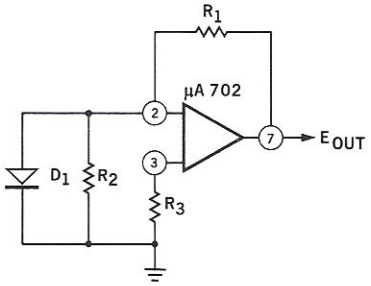
If the amplifier is operating from a DC source resistance less than about 2 K, the offset voltage of the amplifier is the major cause of output offset. In this case, the balancing circuit in Fig. 15a is the best choice. The potentiometer across the inputs (R_4) should be about 20 times greater than the source resistance so that the latter will not contribute to offset. In order to get a smooth adjustment that will null a worst-case unit, R_5 should be determined from

$$\frac{R_2 V^-}{R_5} \simeq 10\,\text{mV}$$

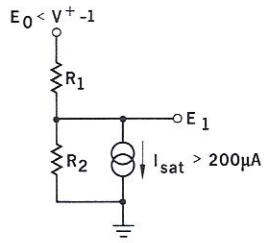
When the amplifier is operating from high DC source resistances such that the offset current is the dominant cause of offset, the zeroing scheme in Fig. 15b will give balance over the widest temperature range. Null will be maintained as long as the percentage difference in the current gains of the input-stage transistors remains constant.

From Fig. 3 it can be seen that if the input voltage on the inverting input terminal exceeds $2V_{BE}$, the input stage transistor will saturate. If this happens, the circuit will still have a gain, but the inverting input will now be a non-inverting input. Therefore, it is important to ensure that large output swings cannot saturate the input stage through the feedback network as this can result in positive feedback and a latch-up condition.

To saturate the input stage, the maximum common-mode voltage on the input terminal must be exceeded, and enough current must be supplied to saturate the input stage (a current nearly equal to the collector current of Q_1 would be required). In general, this is not a problem if the closed-loop gain is greater than 10 or if the feedback resistor between the output and inverting input terminals is greater than 50 K. If there is any question, the latch-up condition can be positively eliminated by connecting a limiting diode between the inverting input terminal and ground as shown in Fig. 16a.



(a) Feedback Circuit and Limiting Diode



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(b) Equivalent Circuit for Latching Condition

FIG. 16. Circuits used to determine whether limiting diode is needed to prevent possible latch-up condition.

If it is desired to determine whether a certain feedback configuration can produce latch-up, the equivalent circuit in Fig. 16b can be used. The maximum output voltage of the amplifier is about 1 V less than the positive supply voltage (V^+), the minimum current that will saturate the input stage is 200 μA, and the minimum input voltage for saturation is 0.5 V. Therefore, sufficient conditions for elimination of latch-up are

$$\frac{R_2 (V^+ - R_1 I_{sat} - 1)}{R_1 + R_2} < 0.5\ \text{V} \tag{17}$$

Frequency Compensation

Because the amplifier will oscillate if the total phase shift reaches 180° while the effective gain is greater than one, some form of frequency compensation is required before feedback can be applied.

The simplest method of providing frequency compensation is to roll off the frequency response of the amplifier with a single RC network. If this rolloff is started at a low frequency, the gain can be made less than unity before any other circuit elements introduce additional phase shift. Since the maximum phase shift associated with a single RC network is 90°, there can be no problem with oscillation.

This approach does not give maximum bandwidth. However, in DC instrumentation applications, frequencies above 100 cps are usually of no concern. It is, in fact, advantageous to kill the high frequency gain of the amplifier to reduce broadband noise and to make the amplifier less susceptible to instability caused by inadequately bypassed supplies, capacitive loading, or stray capacitances in the feedback circuit.

This conservative compensation technique is illustrated in Fig. 17. A large capacitance is placed on the external frequency-compensation pin to roll off the open-loop response at 6 db/octave from approximately 350 cps to 10 Mc. Since it is required that this capacitor behave at frequencies above 10 Mc, a low-inductance ceramic capacitor should be used.

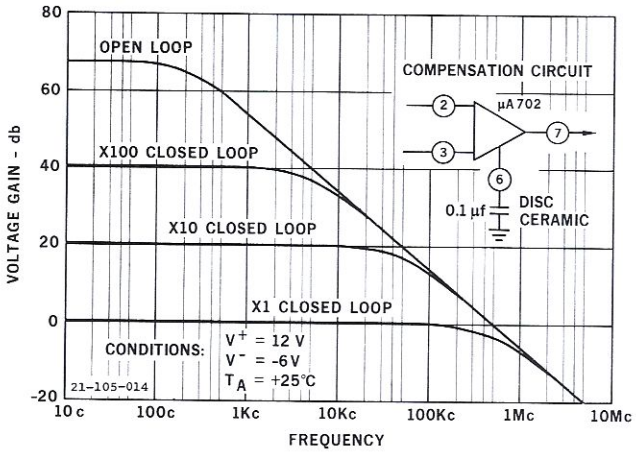

FIG. 17. Compensation circuit for use where maximum bandwidth is unimportant. The frequency response for various gain connections is also given.

It should be noted that, although this circuit gives a bandwidth of nearly 1 Mc with unity gain, full output swing is not available at frequencies in excess of 100 cps. It should also be pointed out that the indicated closed-loop response can vary over a three-to-one range due to variations in open-loop voltage gain, internal resistor values, and compensation capacitor tolerances. However, this will not give rise to instability since the circuit typically has a stability margin in excess of 20 db.

A second compensation technique that gives improved high-frequency performance is shown in Fig. 18. Using this circuit and the indicated design equations, a closed-loop bandwidth of nearly 10 Mc can be realized. Again, with these compensation circuits, full output swing cannot be obtained over the entire frequency range.

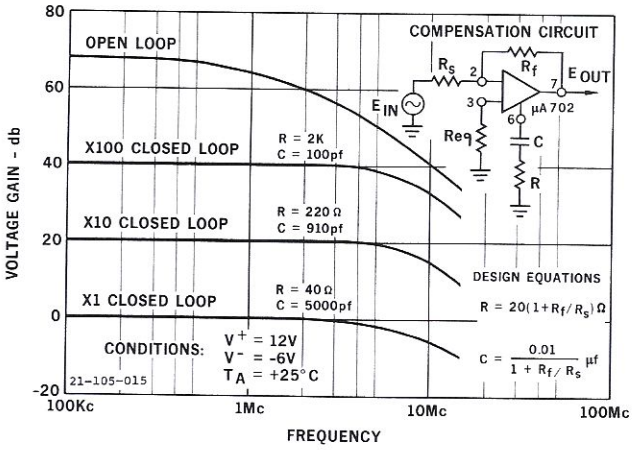

FIG. 18. Frequency response of μA702 compensated for maximum bandwith. The response is given for various closed-loop gain connections. The compensation circuit and design equations are also provided.

With the compensation circuits in Fig. 18, reasonable attention must be given to supply bypassing. It is advisable to bypass the supplies with a low-inductance 0.01-μf capacitor at the device socket or at least within a reasonable distance from the socket. In addition, a certain amount of care must be taken to eliminate stray capacitances in the feedback loop, particularly with the higher gain connections and with high source resistances. If, for example, the feedback resistors are mounted near the amplifier on a printed-circuit board using a neat layout, there should be no problems; however, if the feedback resistors are connected to the device through some length of line or through connectors, a more conservative frequency-compensation technique, such as that in Fig. 17, should be used. Plugboard techniques should be avoided in evaluating any of the connections in Fig. 18.

If full output capability to frequencies approaching 1 Mc and closed-loop bandwidths up to 30 Mc are required, the μA702A should be used with its special compensation techniques.

Typical Circuits

The operational amplifier is a versatile tool in the design of linear circuits. The amplifier has a much wider range of use than as a simple feedback amplifier. Many useful circuits can be found in textbooks on analog-computer techniques, for which the operational amplifier is a basic building block. In what follows, an attempt will be made to indicate the broad scope of applications of this device by specific examples of practical circuits.

Probably one of the largest potential uses for the μA 702 is as a signal conditioner for a telemetry system. One such application is shown in Fig. 19. Here the differential output of a thermistor bridge is amplified by 10. A single-ended output is obtained such that the amplifier output is zero when the bridge is balanced. The high common mode and supply rejection of the amplifier gives null independent of supply voltage. In the circuit shown, the null drift of the bridge due to the amplifier will be less than 3 mV over the temperature range of -55°C to +125°C.

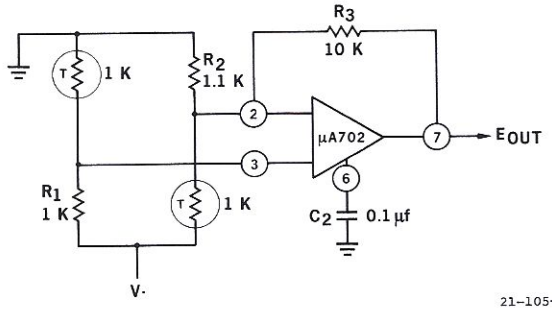

FIG. 19. Amplifier for thermistor bridge.

An amplifier circuit for a piezoelectric transducer is given in Fig. 20. The voltage gain of this circuit is 3, and the input impedance is in excess of 5 MΩ. The lower cut-off frequency of the amplifier, as shown, is 1 cps.

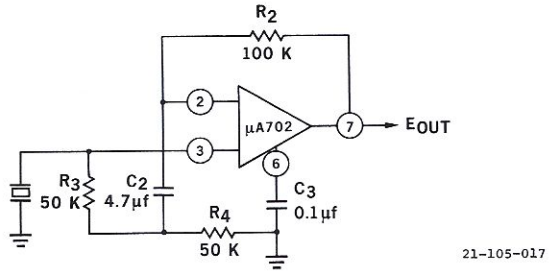

FIG. 20. High input impedance amplifier for piezoelectric transducer.

Figure 21 gives the schematic for a servo preamplifier or position indicator. Solar-cell sensors are used. The circuit shown has a sensitivity of 50 mV/μA. The amplifier responds to the short-circuit output current of the sensors since the voltage across them is kept less than 10 mV.

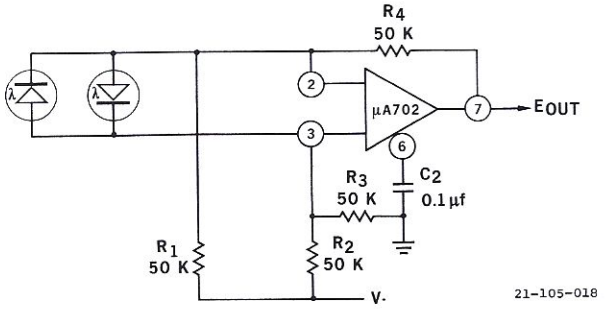

FIG. 21. Preamplifier for servo system using solar cell sensors.

A low-noise preamplifier for use with low-level audio or instrumentation tape heads is shown in Fig. 22. A matched pair of low-noise transistors is used as a differential input stage to provide good common-mode rejection and high input impedance, after which the μA 702 provides amplification. Overall feedback is not employed, but a reasonably constant gain of 100 is provided. With the circuit configuration used, the common-mode range is considerably in excess of that of the μA 702 alone, particularly in the positive direction.

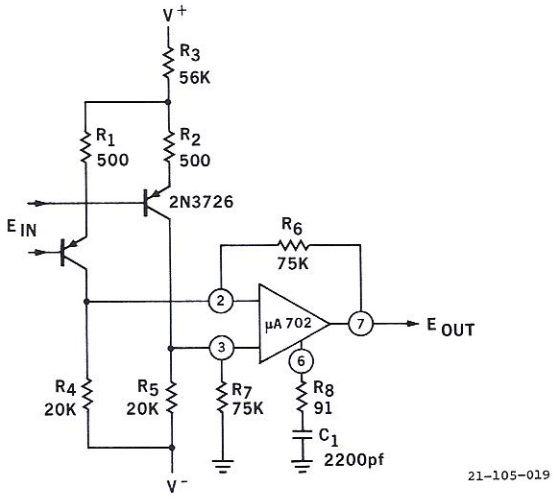

FIG. 22. Low-noise, high input impedance amplifier for use with low-level tape head. Circuit features differential input for noise rejection.

Figure 23 illustrates a light-level sensor using a photodiode as a detector. The circuit as shown functions as a current-operated Schmitt trigger with a 4.0 ±0.1 μA trip level and 0.1 μA hysteresis. The differential-input pair provides higher current resolution than the μA 702 alone. The trip level is determined by R_1, while the hysteresis is governed by the positive feedback from the divider, R_5 and R_6, through R_2. Output drive to a Micrologic gate is provided from the frequency compensation pin. This gives a current-limited drive without the use of clamping diodes.

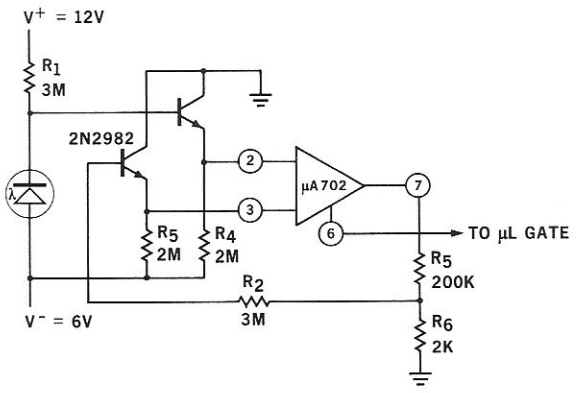

FIG. 23. Photodiode level sensor.

The μA 702 can also be used as an integrator or low-pass amplifier as shown in Fig. 24. The 3-db point in the frequency response will occur for $R_3 = 1/2\pi fC_1$. The capacitor from the noninverting input to ground (C_3) is required in addition to the frequency compensation to eliminate the effect of the input capacitance on that terminal.

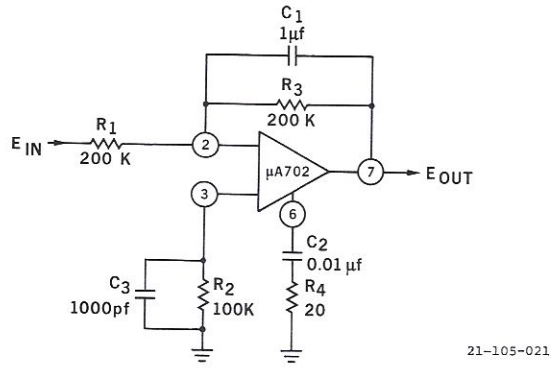

FIG. 24. Integrator or low-pass amplifier.

The use of the μA 702 as a voltage regulator is illustrated in Fig. 25. A temperature-compensated zener diode (D_1) is used to establish a reference for the circuit. An additional emitter-follower transistor is used at the output to deliver a larger output current than can be supplied by the μA 702 alone. Current limiting can be provided by the addition of R_5 and Q_2 as shown in the figure. The output voltage can be made continuously adjustable by installing a potentiometer at the junction of R_3 and R_4. In this application, the μA 702 is operated between +18 V and ground. It is not necessary to make connections to the normal ground terminal (pin 1) since it will normally seek a level of +6 V.

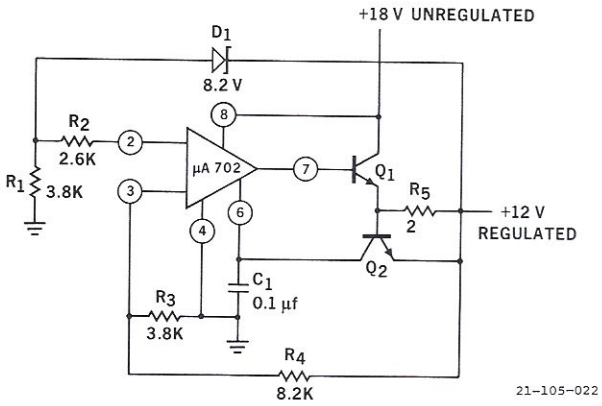

FIG. 25. Temperature-compensated voltage regulator with current limiting.

Frequently in many circuits such as rectifiers, clippers, lampers, and peak detectors where diodes are characteris-ically called for, the threshold voltage of the diode can be significant problem. This is particularly true in low-level ircuits. In these cases an operational amplifier is quite seful in that it can be used to reduce the effective threshold f the diodes by several orders of magnitude.

Figure 26 gives an example of this. It functions as a half-wave rectifier or ideal diode circuit. The output is zero for positive input voltages and an inverted replica of negative input voltages. The threshold voltage of the silicon diodes is divided by the open-loop gain of the amplifier, so it is less than 1 mV.

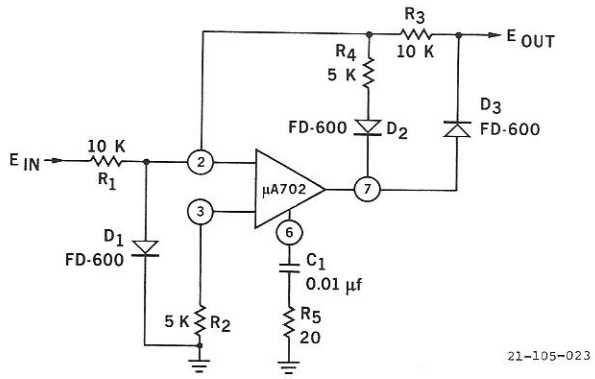

FIG. 26. Half-wave rectifier.

In Fig. 27, the half-wave rectifier is made into a peak detector by the addition of C_3. The output voltage is always positive and equal to the negative peak value of the input waveform.

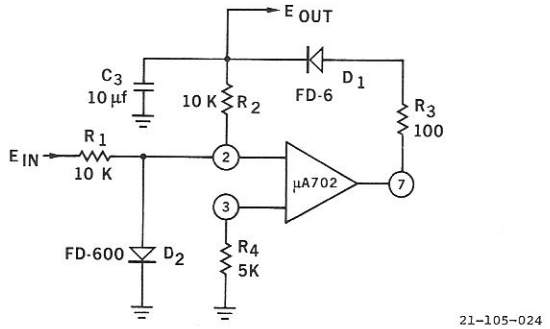

FIG. 27. Peak detector.

Another diode circuit is illustrated in Fig. 28. This is a precision clamper. It gives an inverted, positive-going output signal which is clamped to the DC reference voltage supplied to the amplifier (E_{ref}).

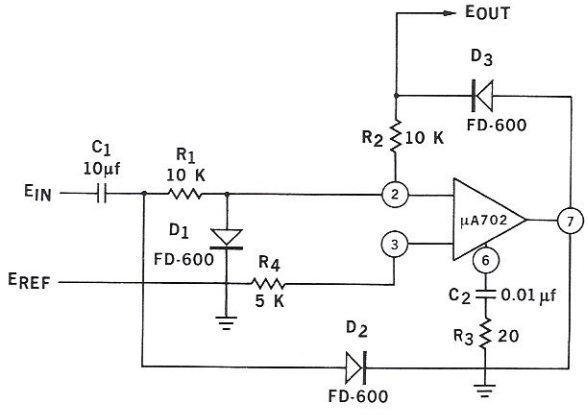

FIG. 28. Clamper.

The circuit in Fig. 29 is another example. The output of the circuit is a positive DC voltage which is proportional to the peak-to-peak value of the input waveform. One precaution is necessary with this circuit: if it is not driven from a low-impedance source, internal frequency compensation is required to prevent oscillations.

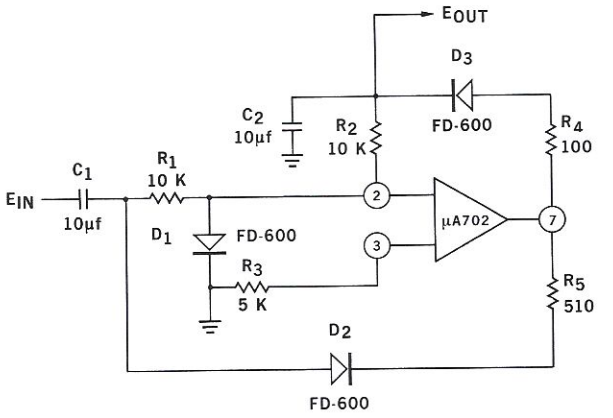

FIG. 29. Peak-to-peak detector.

The last diode circuit to be shown here is the precision full-wave rectifier, or absolute-value generator, shown in Fig. 30. The output is the positive absolute value of the input voltage.

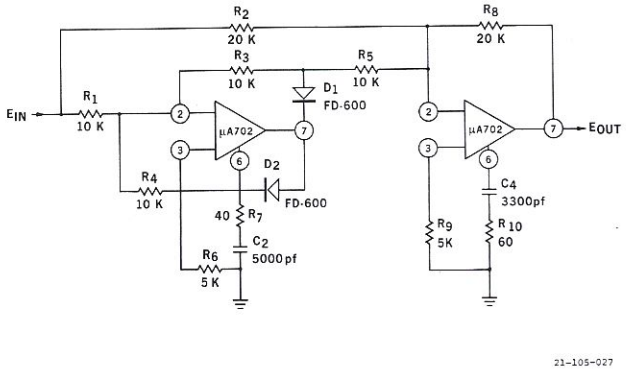

FIG. 30. Full-wave rectifier.

In one particular application, the limited common-mode range of the µA702 does restrict its use when large voltage swings are required. This happens when it is used as a unity gain, noninverting amplifier. The difficulty may be avoided to a certain extent with the circuit in Fig. 31. The common-mode range is actually "bootstrapped" by connecting the output to pin 1. With this circuit, the amplifier may be operated as a voltage follower with output swings of ±3 V.

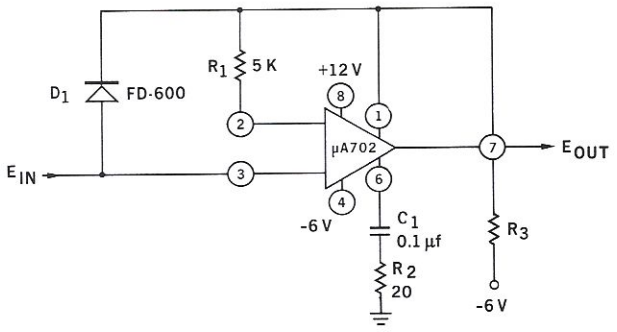

FIG. 31. Voltage follower.

A modified Darlington connection can be used to obtain higher input impedance and lower offset currents than are possible with the µA702 alone. This is shown in Fig. 32. A high-gain, matched transistor pair is used to increase the input impedance. Resistors R_1 and R_2 reduce offset voltage and noise as well as make the gain and open-loop frequency response almost unaffected by the addition of an input stage. A convenient offset null is provided with R_3, although it may be eliminated if not required. It is interesting to note that this method of zeroing offset also minimizes temperature drift. An additional feature of this circuit is that the collector-base diodes of the added transistors serve also as clamping diodes, which prevent driving the amplifier into a latch-up condition by exceeding the common-mode voltage range.

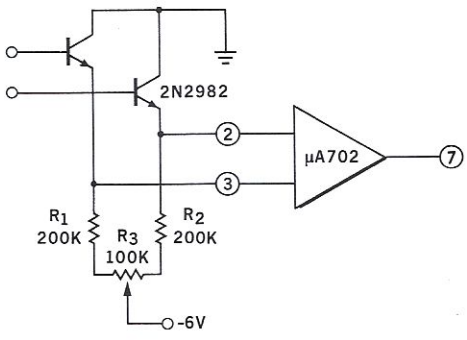

FIG. 32. Circuit for using emitter-follower inputs on the µA702 with a connection which eliminates possible latch-up condition — provisions are also made for balancing offset on the input.

An unusual circuit that further illustrates the broad scope of application of the operational amplifier is the phase detector in Fig. 33. The output is a function of the phase displacement between the signal and reference voltages. Positive and negative outputs are obtained for phase lead and lag.

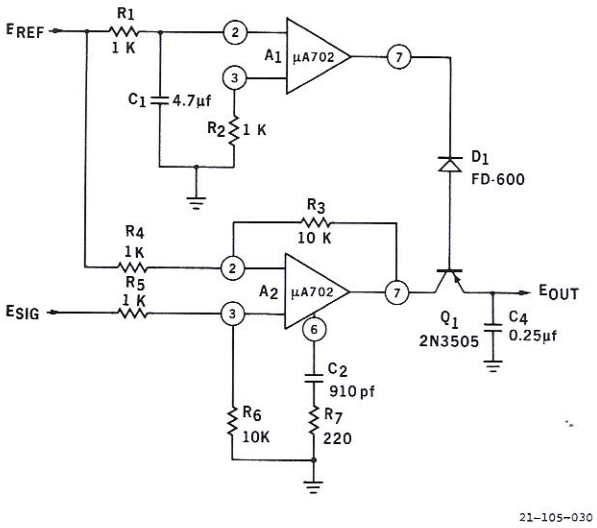

FIG. 33. Transformerless 400-cycle phase detector.

V. TEST CIRCUITS

This section describes a few relatively simple tests that can be used to characterize the amplifier almost completely.

The voltage transfer characteristic yields much useful information about the operation of the amplifier. The gain, linearity, and maximum output swing can be determined from a single oscilloscope trace. A circuit that can be used to display this function is shown in Fig. 34. DC feedback stabilizes the operating point of the amplifier. Capacitors are used to remove the feedback at the test frequency. Solid tantalum capacitors are employed because they have low leakage and provide adequate bypassing at frequencies up to 100 Mc. The amplifier is driven with a triangular waveform through a resistive divider (R_3 and R_4), which eliminates the need for a high-sensitivity horizontal amplifier on the oscilloscope. The amplifier output is DC coupled into the vertical amplifiers.

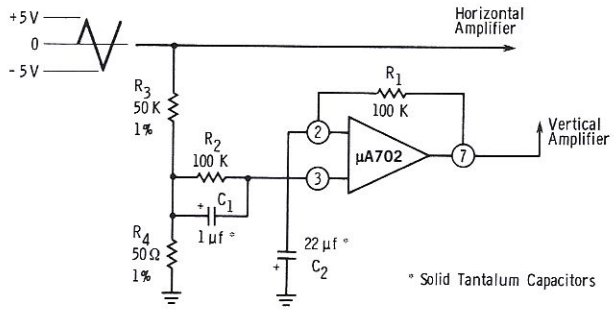

FIG. 34. Circuit for displaying open-loop voltage transfer function on an oscilloscope.

Figure 35 illustrates a convenient method of measuring the offset voltage and current. Precision feedback resistors (R_1 and R_5) are used to fix the amplifier gain at 100. With the switches closed, the amplifier is operating from a very low source resistance (50 Ω) so the voltage on the output will be 100 times the input offset voltage. When both switches are opened, the effective source resistance is increased to 2 K: the change in output voltage will be proportional to the offset current.

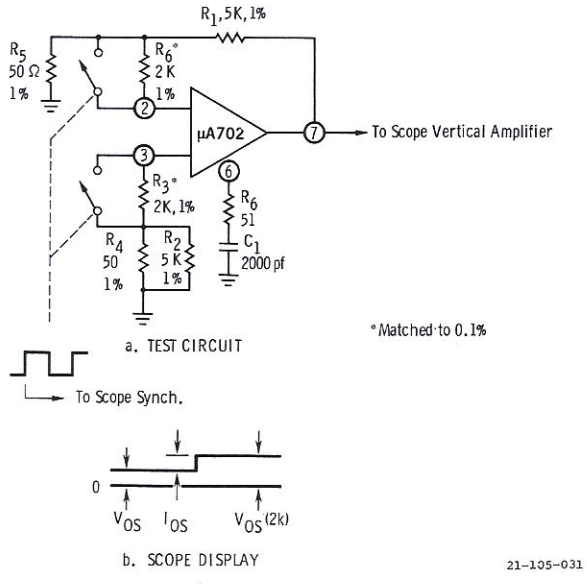

FIG. 35. Circuit for measuring input offset voltage and input offset current.

If an oscilloscope is connected to the amplifier output and its sweep synchronized with the switch driver, the display of Fig. 35 can be obtained. This trace gives the input offset voltage (10 mV/V), the input offset current (5 μA/V), and the effective input offset voltage for a 2-K source resistance (10 mV/V).

The input bias current is easily measured in the circuit of Fig. 36. Since this current is the average of the two input currents, a resistive divider is used to give a direct indication.

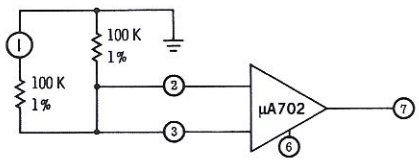

FIG. 36. Circuit for measuring input bias current.

A circuit for measuring the input common-mode rejection ratio is given in Fig. 37. The input terminals are driven over a 4-V range by a 1-Kc input signal. The capacitor and clamping diode limit the positive swing within the operating range of the amplifier. Feedback is used both to stabilize the DC operating point and to fix the gain at 100, which simplifies calculation of the rejection ratio.

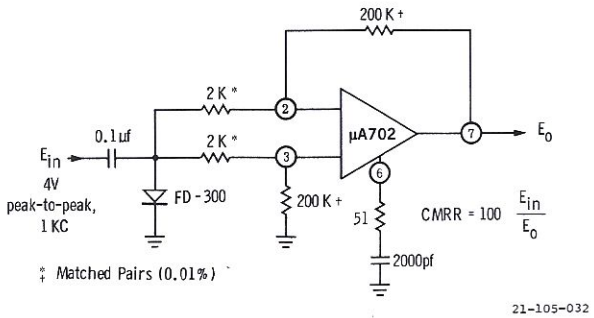

FIG. 37. Circuit for measuring input common mode rejection ratio.